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10/719,801	11/21/2003	Jordan L. Justen	10559/885001/P17580/Intel	3307

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/719,801	JUSTEN, JORDAN L.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in examination of application filed 21 November 2003, in which claims 1 – 30 pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 21 November 2003 was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 – 2, 13 – 15, 16 – 17, and 28 – 30, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1, recites the limitation "a non memory mapped **non-volatile** memory region" in lines 2 on page 10 which contradicts with claimed "non memory mapped **static** memory region" in lines 10 – 11 of claim 1. The terms non-volatile and static are contradictory to each other, which makes the claim indefinite and create confusion,

6. Claim 2, recites the limitation "the memory mapped **static** memory region" in lines 1 – 2 on page 10 which contradicts with claimed memory mapped **non-volatile** memory region of claim 1. The terms non-volatile and static are contradictory to each other, which makes the claim indefinite and create confusion. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 13 – 15 recites the limitation "the another memory" in claims 13 – 15 which creates confusion with the claimed element "another memory region" of claim 10. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 16, recites the limitation "a non memory mapped **non-volatile** memory region" in lines 5 – 6 on page 13 which contradicts with claimed "non memory mapped **static** memory region" in lines 10 – 11 of claim 16. The terms non-volatile and static are contradictory to each other, which makes the claim indefinite and create confusion.

9. Claim 17, recites the limitation "the memory mapped **static** memory region" in lines 1 – 2 on page 14 which contradicts with claimed memory mapped **non-volatile** memory region of claim 16. There is insufficient antecedent basis for this limitation in the claim.

10. Claims 28 – 30 recites the limitation "the another memory" in claims 28 – 30 which creates confusion with the claimed element "another memory region" of claim 25. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1 – 4, and 6 – 9 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shoff et al. [hereinafter as Shoff], US Patent application publication US 2005/0213377 A1.

12. As to claim 1, Shoff, discloses a data processing system [20, computing device, fig. 1], comprising:

a. a memory mapped non-volatile memory region [30, ROM] in including one or more executable instructions [initialization or BIOS code] to initialize [inherent to ROM] the data processing system [20, fig. 1];

b. a non-memory mapped non-volatile memory region [32 NVRAM], the non-memory mapped non-volatile memory region including one or more additional executable instructions [initialization or BIOS code] to initialize the data processing system [20] [para 0039 – 0041 on page 3]; and

c. a memory region [34, RAM] in communication with at least one of the memory mapped non-volatile memory region [30] and the non-memory mapped static memory region [SAT 36, VST 38, Group ID 40][para 0022 – 0025 0n page 2, para 0029 – 0048 on page 3 – 4].

13. As to claim 2, Shoff discloses the non-memory mapped static memory region as a first integrated circuit [34, RAM] including a hardware mechanism [power on or reset] to enable access to the one or more executable instructions [initialization or BIOS code] using a processor memory read [fig. 1].

14. As to claims 3 – 4, Shoff discloses the non-memory mapped non-volatile memory region as a second integrated circuit [32, NVRAM] separate from the first integrated circuit [34][fig. 2] and does not include a hardware mechanism [uses a software] to enable access to the one or more additional executable instructions using a processor memory read [para 00410n page 3].

15. As to claim 6, Shoff discloses the memory region as cache memory [34, RAM].

16. As to claim 7, Shoff discloses the system [20] including a microprocessor [22 processor], and wherein the cache memory [34] is integrated with the microprocessor [22][fig. 1].

17. As to claim 8, Shoff discloses a cache memory [34] is partitioned to include a first region [RAM] to store data and a second region to store one or more pages [SAT 36, VST 38, Group ID 40][fig. 1].

18. As to claim 9, Shoff discloses the cache memory [34, RAM] is partitioned to further include a third region [SAT] to store one or more page [sector] tables [sector allocation tables] [para 0039 on page 3, fig. 1].

19. Claims 1 – 4, and 6 – 9 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Sinclair et al. [hereinafter as Sinclair], US Patent 6,711,059 B2.

20. As to claim 1, Sinclair, discloses a data processing system [20, computing device fig. 1], comprising:

a. a memory mapped [code for start up] non-volatile memory [24, flash memory] region [partitioned] in including one or more executable instructions [start up firmware] to initialize [initialization or configuration] the data processing system [col. 1, lines 64 – 67, col. 2, lines 1 – 5, 47 – 49, fig. 1];

b. a non-memory mapped [pages] non-volatile memory [24, flash memory] region [partitioned], the non- memory mapped non-volatile memory region including one or more additional executable instructions [initialization or BIOS code] to initialize the data processing system [col. 3, lines 13 – 18]; and

c. a memory region [12, SRAM] in communication with at least one of the memory [24, flash memory] mapped [Start up code] non-volatile memory region [partitioned] and the non-memory mapped static memory region [code pages] [col. 3, lines 1 – 67, col. 4, lines 1 – 67, col. 5, lines 18 – 47, col. 6, lines 51 – 67].

21. Claims 1 – 9, and 16 – 24 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Utsumi et al. [hereinafter as Utsumi], US Patent 6,748,527 B1.

22. As to claim 1, Utsumi, discloses a data processing system [col. 4, lines 6 – 8, fig. 1], comprising:

a. a memory mapped non-volatile memory region [memory mapped registers] in including one or more executable instructions [commands] to initialize the data processing system [fig. 2];

b. a non-memory mapped non-volatile memory region [ROM], the non-memory mapped non-volatile memory region including one or more additional executable instructions [initialization or BIOS code] to initialize the data processing system [fig. 2]; and

c. a memory region [RAM] in communication with at least one of the memory mapped non-volatile memory region [memory mapped registers] and the non-memory mapped static memory region [ROM][col. 4, lines 6 – 67, col. 5, lines 11 – 67, col. 6, lines 1 – 28].

23. As to claim 16, Utsumi, discloses a chipset [fig. 2], comprising:

a. a memory mapped non-volatile memory region [memory mapped registers] in including one or more executable instructions [commands] to initialize the data processing system [fig. 2];

b. a non-memory mapped non-volatile memory region [ROM], the non-memory mapped non-volatile memory region including one or more additional executable instructions [initialization or BIOS code] to initialize the data processing system [fig. 2]; and

c. a memory region [RAM] in communication with at least one of the memory mapped non-volatile memory region [memory mapped registers] and the non-memory mapped static memory region [ROM][col. 4, lines 6 – 67, col. 5, lines 11 – 67, col. 6, lines 1 – 28, fig. 2].

24. As to claims 2, and 17, Utsumi discloses the memory mapped memory region as a first integrated circuit [memory mapped registers] including a hardware mechanism

[power on or reset] to enable access to the one or more executable instructions [commands] using a processor memory read [fig. 2].

25. As to claims 3 – 4, and 18 – 19, Utsumi discloses the non-memory mapped non-volatile memory region as a second integrated circuit [ROM] separate from the first integrated circuit [memory mapped registers][fig. 2] and does not include a hardware mechanism [uses a software, code] to enable access to the one or more additional executable instructions [commands/instruction] using a processor memory read [col. 5, lines 11 – 67].

26. As to claims 5, and 20 Utsumi discloses an implementation of memory mapped non-volatile memory region [memory mapped registers] , and non mapped non-volatile memory region [ROM] integrated on a chip, which also includes a flash [fig. 2].

27. As to claims 6, and 22, Utsumi discloses the memory region as cache memory [3, CACHE memory][fig. 1].

28. As to claims 7, and 21, Utsumi discloses the data processing system [fig. 1] including a microprocessor [10 processor], and wherein the cache memory [3] is integrated with the microprocessor [10] including communication with chipset [fig. 1].

29. As to claim 8 – 9, and 23 – 24, Utsumi discloses a cache memory [3] and control section, which inherently teaches partitioning to include a first region to store data and a second region to store one or more pages [fig. 1].

30. Claims 10 – 15, and 25 – 30 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Gibson et al. [hereinafter as Gibson], US Patent 6,601,167 B1.

31. As to claim 10, Gibson discloses a method of initializing a computer system [10, fig. 1, 4], comprising:

a. accessing memory mapped firmware [first portion of boot code] using a processor memory read [read command][col. 2, lines 25 – 29, col. 3, lines 57 – 59, fig. 4];

b. executing an instruction [copy instruction] included in the memory mapped firmware [first portion of boot code] [col. 2, lines 31 – 33];

c. copying [copying] a page [second portion] including another instruction [boot code] from non-memory mapped firmware to another memory region [RAM]; and

d. executing the another [branch (jump)] instruction [col. 2, 25 – 49, col. 3, lines 45 – 67, col. 4, lines 1 – 21, fig. 4].

32. As to claim 25, Gibson discloses an article of manufacture comprising a machine readable medium [32 memory] containing code having instructions [boot code] that, when executed, cause the machine [computer, fig. 1] to:

a. accessing memory mapped firmware [first portion of boot code] using a processor memory read [read command][col. 2, lines 25 – 29, col. 3, lines 57 – 59, fig. 4];

b. executing an instruction [copy instruction] included in the memory mapped firmware [first portion of boot code] [col. 2, lines 31 – 33];

c. copying [copying] a page [second portion] including another instruction [boot code] from non-memory mapped firmware to another memory region [RAM]; and

d. executing the another [branch (jump)] instruction [col. 2, 25 – 49, col. 3, lines 45 – 67, col. 4, lines 1 – 21, fig. 4].

33. As to claims 11, and 26, Gibson discloses a method for initializing a computer system with boot program including actions a through d, which are performed prior to initializing a main memory [inherent to boot process] of computer system.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

34. Claims 12, and 27, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al. [hereinafter as Gibson], US Patent 6,601,167 B1 as applied to claims 10 - 11, and 25 - 26 above, and further in view of Avraham, US Patent application publication 2003/0233533 A1.

35. As to claims 13 – 15 and 28 – 30, Gibson discloses

36. As to claims 12, and 27, Gibson discloses a system and method of initializing a computer system [10, fig. 1, 4], accessing memory mapped firmware [first portion of boot code] using a processor memory read [read command][col. 2, lines 25 – 29, col. 3, lines 57 – 59, fig. 4]; executing an instruction [copy instruction] included in the memory mapped firmware [first portion of boot code] [col. 2, lines 31 – 33]; copying [copying] a page [second portion] including another instruction [boot code] from non-memory mapped firmware to another memory region [RAM]; and executing the another [branch (jump)] instruction [col. 2, 25 – 49, col. 3, lines 45 – 67, col. 4, lines 1 – 21, fig. 4].

However, Gibson does not teach initializing at least a portion of cache memory as random access memory [RAM].

Avraham discloses a method of booting a computer system form cache memory included in processor with steps of loading boot code into cache memory, and executing the boot code that is loaded in cache memory by processor including initializing at least portion of cache memory converted into RAM [para 0008 – 0010 on page 1].

It would have been obvious to one of ordinary skill in art, having the teachings of Gibson and Avraham before him at the time of invention was made, to modify the initialization method for computer system as disclosed by Gibson to include booting from cache as taught by Avraham in order to obtain a computer system boots itself by loading and executing boot code in its processor's cache memory [para 0001 on page 1] and make execution of code faster [para 0001, 0003 on page 1], one of ordinary skill in the art wanted to be motivated to make execution of code faster [para 0001, 0003 on

page 1], and computer lacks a boot code ROM instead a processor includes a small read-only memory [ROM] to store a small part of boot code [para 0006 on page 1].

37. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

38. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin C. Patel
May 24, 2006

A. ELAMIN
PRIMARY EXAMINER